WHAT IS CLAIMED IS

1. A method of fabricating an exposure mask for semiconductor manufacture comprising the steps of:

forming a chrome layer, a first photo resist, a conductive layer and a second photo resist on a transparent quartz substrate, in sequence;

forming a second photo resist pattern by exposing and developing the second photo resist;

forming a conductive layer pattern by etching the conductive layer using the second photo resist pattern as an etch barrier;

removing the second photo resist pattern;

forming an oxide layer as a layer for shielding light at a surface of the conductive layer pattern by oxidizing the conductive layer pattern;

exposing the first photo resist using the conductive layer pattern having the oxide layer at the surface thereof;

forming a first photo resist pattern exposing parts of the chrome layer by developing the exposed first photo resist;

forming a mask pattern including the chrome layer by selectively etching the exposed chrome layer parts; and

removing the conductive layer pattern including the oxide layer and the first photo resist pattern.

2. The method of fabricating an exposure mask for semiconductor manufacture according to claim 1, wherein the conductive layer is an Ag layer.

3. The method of fabricating an exposure mask for semiconductor manufacture according to claim 2, wherein the Ag layer is formed to a thickness of 500 to 3,000Å by using sputtering or MOCVD process.

4. The method of fabricating an exposure mask for semiconductor manufacture according to claim 2, wherein the oxide layer is an Ag oxide layer (AgO_X).

5. The method of fabricating an exposure mask for semiconductor manufacture according to claim 4, wherein the oxidation process of the Ag layer is performed at a temperature of 200 to 300°C at a pressure of 500 to 1,000 mTorr for 100 to 150 seconds by using O_2 or O_3 plasma.

6. The method of fabricating an exposure mask for semiconductor manufacture according to claim 1, wherein the second

photo resist is exposed by using a high voltage E-beam or focused ion beam as a light source.

7. The method of fabricating an exposure mask for semiconductor manufacture according to claim 1, wherein the first photo resist is exposed by using G-line (λ=436nm), I-line (λ=365nm) or KrF(λ=248nm) as a light source.

8. The method of fabricating an exposure mask for semiconductor manufacture according to claim 1, wherein the conductive layer pattern including the oxide layer is removed in accordance with a dry etching process using Cl_2BCl_3 gas.

9. The method of fabricating an exposure mask for semiconductor manufacture according to claim 1, wherein the first photo resist pattern is removed by using O_2 ashing.

10. The method of fabricating an exposure mask for semiconductor manufacture according to claim 1, further comprising the step of cleaning the mask pattern, after the conductive layer pattern including the oxide layer and the first photo resist pattern are removed.